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(22) The substrate wafer may be of sapphire or silicon, and the multilayer metal-polymer dielectric structure may define a plurality of passive elements, such as resistors, capacitors inductors and transformers for terminating, matching, filtering, biassing, energising or performing other functions in relation to the device under test.

DRAWING DESCRIPTION:

BRIEF DESCRIPTION OF THE DRAWINGS

A structure for testing bare integrated circuit devices in accordance with the present invention will now be described by way of example with reference tc the drawing, of which:

FIG. 1 shows schematically a part of the structure in section, and

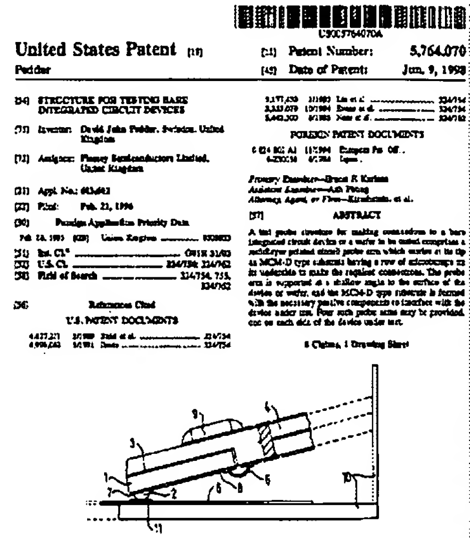
FIG. 2 shows schematically a part of the structure in plan view.

DETAILED DESCRIPTION:

(1) DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

(2) Referring first to FIG. 1, the structure comprises a small multichip module (MCM-D) substrate 1, a multilayer metal-polymer dielectric structure on an insulating wafer, which is provided with contact microbumps 2 and bonded, by means of a thermoplastic adhesive 3 to a multilayer printed circuit board, angled probe structure 4. Connections between the substrate 1 and the printed circuit board tracks that lead to external test circuitry (not shown) are made by means of short wire bond links 5 that are physically clear of the surface of the device 6 under test as a result of the angled probe arrangement. As shown in FIG. 2, one such probe 4 is employed for each side of the device under test, each probe 4 being presented to the device 6 under test at a shallow angle. The substrate 1 comprises a sapphire, fused quartz or silicon wafer on which is defined a multilayer metal-polymer dielectric interconnect structure that provides power, ground and signal interconnect functions and integrated thin film passive components that include resistors, capacitors and inductors. This structure is compatible with in-situ ink marking of defective devices immediately after test, through the aperture defined between the tips of the probes 4.

(3) The substrate 1 may be produced by known processes, to provide for example a three layer aluminium metallisation and polyimide dielectric structure, together with a full range of integrated passive components. The track geometries on the substrate 1 are between 10 and 25 micrometer line widths, with metal thicknesses of 2 to 5 micrometers at track pitches of 40 to 100 micrometers, while dielectric thicknesses are in the 5 to 20 micrometer range. Such geometries allow controlled impedance, 50 ohm lines to be defined


United States Patent

Pedder

Patent Number: 5,764,070

Date of Patent: Jun. 9, 1998

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ASSIGNEE-INFORMATION:

NAME	COUNTRY
NIPPON OIL & FATS CO LTD	N/A

APPL-NO: JP02064091

APPL-DATE: March 16, 1990

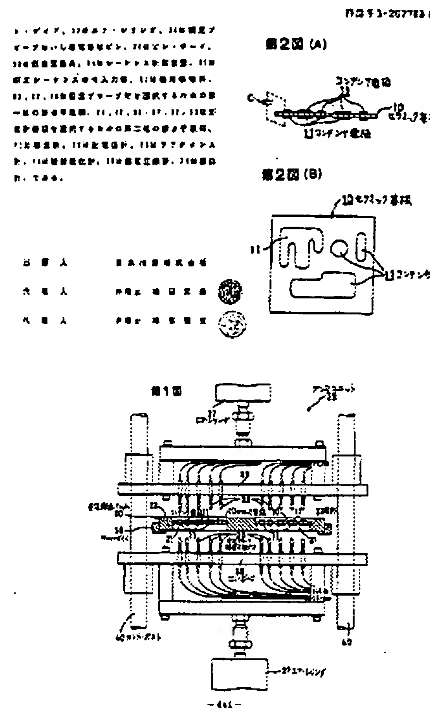
INT-CL (IPC): G01R001/073, G01R027/00

US-CL-CURRENT: 324/754

ABSTRACT:

PURPOSE: To contrive a reduction of measurement processing time by providing groups of contact means electrically connecting only a pair of measuring probes in contact with a pair of terminal electrode patterns of plural capacitors to the measuring input of a selected meter among a group of meters.

CONSTITUTION: As a board tester for the capacitor incorporated substrate 10, at least a capacitance meter 71, withstand voltage meter 72, reactance meter 73, insulating-resistance meter 74, and withstand voltage tangent meter 75 are provided. By a sequence control device 51, opening and closing states of each contact of a 1st class contacts group 61-63 for selecting a capacitor C to be measured at present among the plural capacitors C and a 2nd class contacts group 64-69 to changeover the measuring meters according to the measuring items, are controlled in accordance with a settled instruction sequence. For instance, when the contact 61 only is closed by the device 51, a most left capaci tor C on the substrate 10 is selected. When only the contact is closed further, only a pair of measuring probes 38 in contact with a pair of electrode patterns 11 of the selected capacitor C are connected to the measuring input of capaci tance meter 71, and the capacitance value of selected capacitor C is measured by the capacitance meter 71.



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HIROSE, EIICHIRO
INUI, SHINICHIRO

ASSIGNEE-INFORMATION:

NAME	COUNTRY
MITSUBISHI MATERIALS CORP	N/A

APPL-NO: JP04134546

APPL-DATE: May 27, 1992

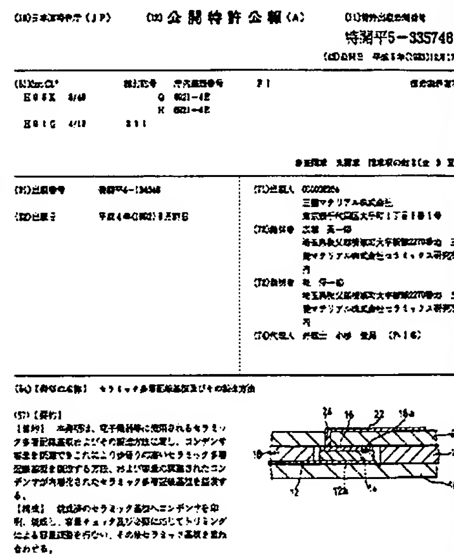
INT-CL (IPC): H05K003/46, H01G004/12

US-CL-CURRENT: 29/835

ABSTRACT:

PURPOSE: To adjust capacitance, and manufacture a ceramic multilayer wiring board having a high yield by providing a trimmed capacitor on an inner layer sandwiched between a number of ceramic substrates.

CONSTITUTION: A capacitor upper electrode 16 with one side thereof formed into a comb tooth shape is printed on an upper part of a dielectric material 14, and it is calcined after having been dried. A probe is brought into contact with an area between a capacitance check pad 12b of a lower electrode 12a and the electrode 16 to check the capacitance of the capacitor. When the capacitance is outside of a tolerance, the upper electrode 16 is trimmed by a laser beam or the like, so that a trimmed portion 16a is formed. Thereafter, joint glass 18 is printed on a substrate, and an alumina substrate 20 is laminated on the glass. This laminated substrate is then calcined. Thereby, it is possible to manufacture with a high yield a ceramic multilayer wiring board on which a capacitor with its capacitance prepared is mounted.



for terminating the low impedance line. The first combination of R.sub.1 C.sub.1 and L.sub.1 acts to terminate the line at extremely high frequencies, e.g., in the region of 10 GHz, and consequently inductance L.sub.1 must be extremely low. The second combination of R.sub.2 C.sub.2 and L.sub.2 is effective at slightly lower frequencies and C.sub.2 is very large, on the order of 0.01 microfarads. The whole network is effective as an all-pass network and takes the place of a single bypass capacitor over a frequency range of interest, without introducing excessive reactive components, while terminating the low impedance line in satisfactory manner.

(5) In the circuit of FIG. 4, L.sub.1 is minimized, C.sub.2 is maximized and (L.sub.2 /C.sub.1).sup.1/2 =four ohms. L.sub.1 is minimized by providing extremely short leads for R.sub.1 and C.sub.1, the latter comprising a "gap-cap" capacitor. R.sub.1 is printed under the gap in the mounting pads or the "gap-cap" capacitor in a manner to be described in connection with FIG. 5. The second half of the split-band all-pass network suitably embodies the 0.01 microfarad capacitor C.sub.2 as a ceramic chip cap, and L.sub.2 is just the parasitic inductance encountered in connecting C.sub.2.

(6) Referring to FIG. 5, illustrating more fully the first part of the all-pass network, this circuit is desirably implemented on the same alumina substrate 20 as the probe at a point remote from the tip end of the board, where sufficient space is available. The power conductor 26 at the end thereof remote from the board tip is superimposed by gap-cap capacitor 44 forming C.sub.1. The gap-cap capacitor includes conducting layer 46 bridging underlying metal layers 50 and 52 and separated therefrom by thin dielectric layer 48. A layer of silver epoxy 54 joins power conductor 26 to layer 50 of the capacitor, it being understood the power conductor 26 is supported on polyimide layer 40 above ground conductor 24 on substrate 20. Layer 52 of the capacitor is connected by way of silver epoxy 56 to a conductive layer 58 disposed in a via in the polyimide for making contact with conductor 60 forming part of the first layer metal of the device but isolated from grounded portions of the first layer metal. The resistor R.sub.1 for the circuit comprises a printed resistive layer 42 on the alumina substrate for making connection between metal conductors 24 and 60. The inductance (L.sub.1) of the circuit is extremely low and substantially constitutes the inductance of the contacts. The second half of the all-pass network in FIG. 4 is implemented in a somewhat more conventional manner with the higher capacitance and wherein a slightly larger lead inductance, L.sub.2, can be tolerated.

(7) FIG. 6 is a more detailed illustration of a portion of a wafer probe according to the present invention, wherein reference numerals correspond substantially to those used in FIGS. 2 and 3. In the illustrated embodiment of FIG. 6, eight signal conductors 22 extend to connections 32 at the tip end of the probe board, while the power conductors 26, forming the lower impedance lines, are interspersed therebetween. In this view, various terminating connections and resistances are illustrated. The nomenclature for the types of

U.S. Patent Aug. 16, 1988 Sheet 5 of 6 4,764,723

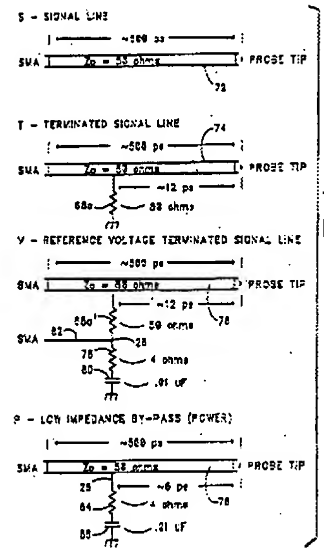


FIG.7

INVENTOR-INFORMATION:
NAME
MIZUTA, MASAHARU

ASSIGNEE-INFORMATION:

NAME	COUNTRY
MITSUBISHI ELECTRIC CORP	N/A

APPL-NO: JP09228079

APPL-DATE: August 25, 1997

INT-CL (IPC): G01R001/073, H01L021/66

ABSTRACT:

PROBLEM TO BE SOLVED: To reform the surface at the forward end of a probe uniformly by forming a probe part to be connected electrically with a substrate part arranged with the probe and the substrate part incorporating electronic components removably.

SOLUTION: A substrate part 7 comprises a printed board 7a mounting electronic components, e.g. a resistor or a capacitor. The basic material of a plurality of probes 9 has one end made of tungsten, for example, forming a contact part 9a with the pattern on the printed board 7a and the other end forming a forward end part 9b touching the electrode on a substrate to be inspected, i.e., a wafer. A conductive rubber member 10 is interposed between the pattern on the printed board 7a and the contact part 9b of the probe 9 and conducts them electrically. A fixing screw 12 fixes a holding frame 11 at a specified position of the substrate part 7 and presses the conductive rubber member 10 against the pattern on the printed board 7a from the contact part 9a of the probe 9 through the holding frame 11. A probe 13 is composed of the components from the probes 9 to the fixing screws 12.